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An Organic/Si Nanowire Hybrid Field Configurable Transistor

Qianxi Lai,[†] Zhiyong Li,[‡] Lei Zhang,[†] Xuema Li,[‡] William F. Stickle,[§] Zuhua Zhu,[†] Zhen Gu,[†] Theodore I. Kamins,[‡] R. Stanley Williams,[‡] and Yong Chen*[,†]

Department of Mechanical and Aerospace Engineering and California NanoSystems Institute, University of California, Los Angeles, California 90095, Quantum Science Research, Hewlett-Packard Laboratories, 1501 Page Mill Road, Palo Alto, California 94304, and Advanced Materials Process Lab and Advanced Diagnostic Lab, Hewlett-Packard Company, Corvallis, Oregon 97330

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ABSTRACT

We report a field configurable transistor (FCT) fabricated on a Si nanowire FET platform by integrating a thin film of conjugated polymer poly[2-methoxy-5-(2′-ethylhexyloxy)-*p*-phenylene vinylene] (MEH-PPV) and an ionic conductive layer ($RbAg_4I_5$) into the gate. The FCT can be precisely configured to desired nonvolatile analog state dynamically, repeatedly, and reversibly by controlling the concentration of iodide ions in the MEH-PPV layer with a gate voltage. The flexible configurability and plasticity of the FCT could facilitate field-programmable circuits for defect-tolerance and synapse-like devices for learning.

The continued miniaturization of the Si-based field-effect transistor (FET) will reach its fundamental physical limit in a decade or so,[1] which has led to significant efforts in the development of new nanoscale electronic devices based on Si nanowires,[2] carbon nanotubes,[3] molecules,[4] etc. Simple electronic circuits based on these nanodevices[5–7] have also been demonstrated, but it is challenging to integrate these devices into large-scale functional circuits for practical applications due to the inevitable defects introduced during the fabrication of these devices and circuits. Various defect-tolerant circuit architectures have been proposed,[8–11] in which the defects in circuits can be identified by postfabrication tests, and then the defects can be corrected and the circuits can be reconfigured toward desired functions. To build up the defect-tolerant circuit, it is highly desirable to develop nanoscale field configurable devices that can not only preserve the merits of the Si FET but also incorporate synapse-like analog configurability and plasticity. Floating gate Si FETs have been used for digital field programmable circuits, but such devices can hardly be integrated with nanowire-based devices and are difficult to configure precisely to a desired analog state.[12] Recently, organic molecules were incorporated into the gate structures of Si FETs[13] and semiconductor nanowire transistors,[14,15] which can then be configured to bistable or multiple discrete electronic states by applying a gate voltage to control the redox state of the molecules. Although these devices have been demonstrated for multiple-state nonvolatile memory and programmable logic applications, it is difficult to integrate a liquid electrolyte into a gate structure or semiconductor nanowires with back gates into more general-purpose circuits.

In this letter, we report an organic/Si hybrid field-configurable transistor (FCT) fabricated on a Si nanowire FET platform that can be flexibly configured to precise analog states. The device structure is shown schematically in Figure 1a. A thin film of poly[2-methoxy-5-(2′-ethylhexyloxy)-*p*-phenylene vinylene] (MEH-PPV), a conjugated polymer, and an inorganic layer of $RbAg_4I_5$, an ionic conductor,[16] were sandwiched between the gate SiO_2 layer and an Al/Ti metal gate electrode to incorporate the configuration function. When a gate voltage exceeding a threshold value is applied, depending on its polarity, the iodide ions from the $RbAg_4I_5$ are injected into or extracted from the MEH-PPV layer, resulting in the configuration of the FCT electronic characteristics.

The FCT preserves the conventional Si source−channel−drain (n−p−n) structure. The FET Si nanowire channel is p-Si with a nominal boron doping concentration of $3 \times 10^{17}/cm^3$ and has a width of 80 nm, a thickness of 60 nm, and a length of 10 μm, respectively. A scanning electron microscope (SEM) image shows its structure in Figure 1b. The n-Si source and drain had a nominal phosphorus doping concentration of $1 \times 10^{20}/cm^3$. The source and drain patterns were fabricated by photolithography, and the nanoscale Si channel was fabricated by e-beam lithography on a Si layer

* Corresponding author. E-mail: yongchen@seas.ucla.edu.
† University of California, Los Angeles.
‡ Hewlett-Packard Laboratories.
§ Hewlett-Packard Company.

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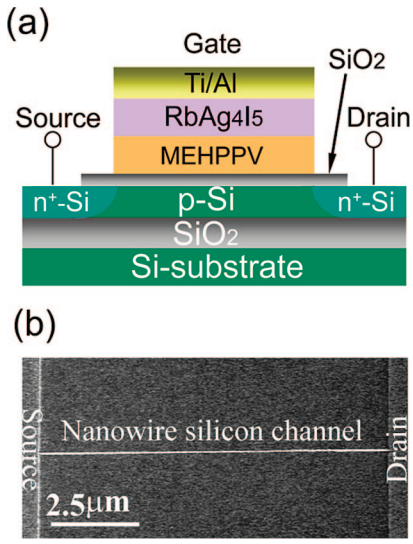

Figure 1. (a) Schematic showing the structure of a polymer/Si nanowire hybrid field-configurable transistor. (b) SEM image showing the SOI-based Si nanowire channel region.

on a silicon-on-insulator (SOI) wafer. A 3 nm thick gate SiO_2 insulating layer was prepared by thermal oxidation to cover the Si nanowire channel. A layer of MEH-PPV with a thickness of 60 nm was spin-coated on top of the SiO_2 insulating layer. A 60 nm thick $RbAg_4I_5$ ionic conducting layer was deposited on the top of the MEH-PPV polymer layer by thermal evaporation of a powder mixture of 82 mol % AgI and 18 mol % RbI. Finally, a metal gate electrode consisting of a 20 nm thick Ti layer followed by an 80 nm thick Al layer was deposited by electron-beam evaporation. The MEH-PPV polymer beyond the gate electrode area was etched away with an O_2 plasma using the gate metal electrode as an etching mask. Conventional Si FETs (without the $RbAg_4I_5$/MEH-PPV bilayer in the FCT gate shown in Figure 1a) were also fabricated as control devices by using the same process as described above, except that the steps to integrate the $RbAg_4I_5$/MEH-PPV bilayer were omitted. The test results of the control FETs demonstrated decent transistor characteristics, which are included in the Supporting Information.

All FCTs were measured at room temperature under vacuum ($<10^{-4}$ Torr) in a Desert Cryogenics vacuum probe station to prevent oxygen and moisture from contaminating the ionic/organic bilayer. The electrical measurements of the FCT and the control FET devices were carried out using a HP4156B semiconductor parameter analyzer, an Agilent 31220 wave function generator, and a Fluke 199B oscilloscope. Typical source−drain current (I_d) versus gate−source voltage (V_g) characteristics of the FCTs with a drain−source voltage $V_d = 1$ V and a grounded source are shown in Figure 2a for different configuration states. Curve **1** in Figure 2a shows an I_d–V_g characteristic for a FCT in its initial state with a threshold voltage $V_T \approx 1.0$ V. After sweeping a large positive configuration voltage V_g from 0 → 7 V within 3.5 s, the threshold voltage changes to $V_T = -1.0$ V (curve **2**); after sweeping a negative configuration voltage V_g from 0 → −5 V, $V_T = 4.0$ V (curve **3**). The ratio of I_d for a FCT measured at state **2** ($V_T = -1.0$ V) to that measured at state **3** ($V_T = 4.0$ V) was more than 10^6 when tested at $V_g = 0.5$ V and $V_d = 1$ V. More than 30 FCTs have been fabricated and tested separately. Before configuration, the original threshold voltages of the as-fabricated FCTs were distributed between 1 and 2 V. After sweeping a configuration voltage V_g from 0 → 7 V or 0 → −5 V, the threshold voltages of the FCTs were configured to -1.0 ± 0.2 V and 4.0 ± 0.2 V, respectively. The wide configuration range of the gate threshold voltages (−1.0 to 4.0 V) and the large configuration ratio of the source−drain currents (up to 10^6) provides the flexibility to configure FCTs to a wide range of desired characteristics in a field configurable circuit. After configuration, the V_T remained stable for a long retention time when it was tested with $|V_g - (V_d + V_s)/2| < 1.5$ V, as discussed below.

The FCTs can be configured to arbitrary states dynamically and reversibly by applying a series of V_g pulses with different amplitude, polarity, and duration. A series of negative configuration V_g pulses with a fixed amplitude $V_g = -4$ V and a duration of 100 ms was applied to the FCT. After each pulse, the FCT was stabilized at $V_g = 0$ V for 100 ms, and then I_d was measured at $V_g = 1$ V and $V_d = 1$ V. As shown in Figure 2b, I_d was progressively decreased by the negative configuration V_g pulses. When a series of positive configuration V_g pulses with an amplitude $V_g = 5$ V and a duration of 10 ms was applied, the process described above was reversed. After each pulse, the FCT was stabilized at $V_g = 0$ V for 10 ms, and then I_d was measured at $V_g = 1$ V and $V_d = 1$ V. As shown in Figure 2c, I_d was progressively increased by the positive configuration V_g pulses. The results indicate that the FCT can be gradually tuned by low amplitude configuration voltages that are compatible with CMOS circuits.

The configuration rate of the FCT can be modified by the amplitude of the configuration gate voltages. To study this effect, V_T in a FCT was first configured to its minimum value by applying a positive configuration voltage $V_g = 7$ V with extensive duration, and then I_d was sequentially decreased by a series of V_g pulses with a fixed duration of 100 ms and fixed amplitudes of −6, −5, −4, −3, and −2 V, respectively. The change of the FCT threshold voltage ΔV_T was derived from the change of I_d and is shown in Figure 2d as a function of the number N_p of the applied V_g pulses. The configuration rate, $d\Delta V_T/dN_p$, increased significantly when the amplitude of V_g pulses increased from −2 to −6 V. In a similar fashion, V_T in a FCT was first configured to its maximum value by applying a negative configuration voltage $V_g = -6$ V with extensive duration and then I_d was sequentially increased by a series of V_g pulses with a fixed duration of 100 ms and fixed amplitudes of 2, 3, 4, 5, and 6 V, respectively. The change of the FCT threshold voltage ΔV_T was derived from the change of I_d and is shown in Figure 2e as a function of the number N_p of the applied V_g pulses. The configuration rate, $d\Delta V_T/dN_p$, increased significantly when the V_g pulse increased from 2 to 6 V.

The FCT can be dynamically configured to a targeted state precisely by a closed-loop feedback control circuit (the details of the circuits are described in the Supporting Information).

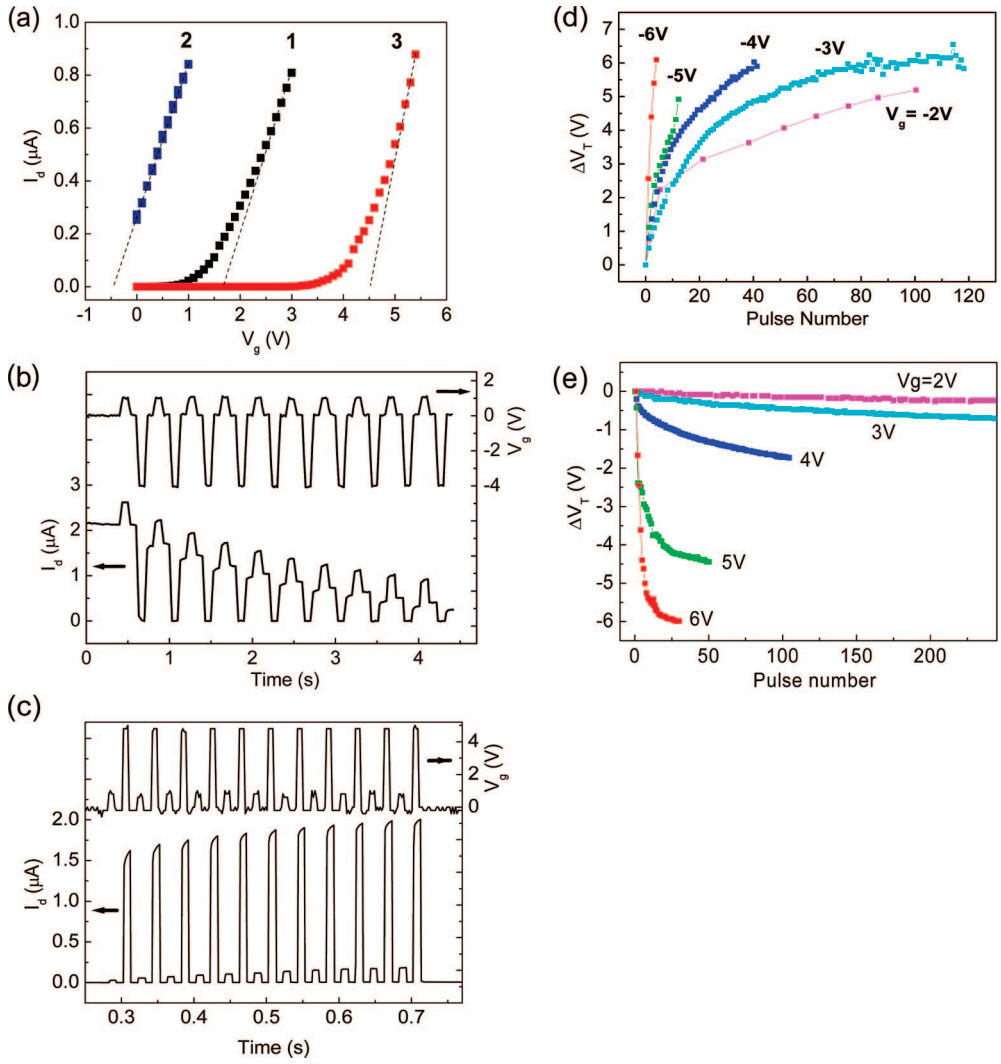

Figure 2. (a) I_d−V_g data (symbols) measured for the initial state before configuration (curve 1), after sweeping V_g from 0 → 7 V (curve 2), and after sweeping V_g from 0 → −5 V (curve 3). The intercept with the V_g axis of the dashed straight line tangent to the I_d–V_g data points determines the transistor threshold voltages (V_T + (V_d + V_s)/2) for each configured state. (b) I_d (lower curve) is progressively decreased by applying a series of negative configuration V_g pulses with an amplitude V_g = −4 V (upper curve). (c) I_d (lower curve) is progressively increased by applying a series of positive configuration V_g pulses with an amplitude V_g = 5 V (upper curve). (d) The change of the threshold voltage V_T is plotted (data points) as a function of the number of negative configuration gate voltage pulses, N_p, for fixed amplitudes V_g = −6 V (red), −5 V (green), −4 V (deep blue), −3 V (sky blue), and −2 V (magenta). (e) The change of the threshold voltage V_T is plotted (data points) as a function of the number of positive configuration gate voltage pulses, N_p, for fixed amplitudes V_g = 6 V (red), 5 V (green), 4 V (deep blue), 3 V (sky blue), and 2 V (magenta).

During the configuration, I_d was measured and compared continuously with a target reference current I_{ref}, which was preset by the training circuit. If I_d was higher or lower than I_{ref}, negative or positive V_g pulses, respectively, were applied to the FCT to reduce the difference, $|I_d - I_{ref}|$. The V_g pulses were kept at a fixed duration of 10 μs and a fixed amplitude of V_g = 8.5 V when $I_d < I_{ref}$ or −5.5 V when $I_d > I_{ref}$, but the number of applied V_g pulses was set by the training circuit to be linearly proportional to $|I_d - I_{ref}|$ to adjust the configuration rate automatically. The reading, comparison, and configuration occurred continuously and simultaneously. The high-frequency transient currents induced by the configuration V_g pulses were filtered out. As shown in Figure 3, I_{ref} was set to different values in the range 0.25–4.5 μA, and I_d was automatically configured to follow the change of I_{ref} by applying the configuration V_g pulses. The configuration

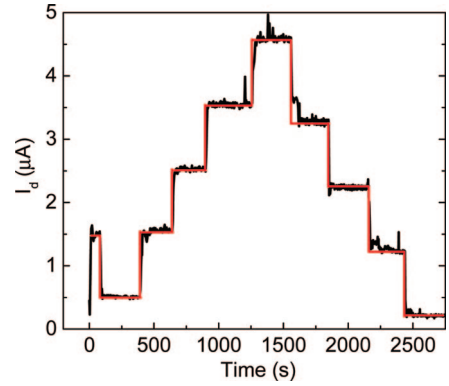

Figure 3. Source−drain current, I_d (black line) is automatically configured by a closed-loop feedback control circuit to various target reference currents, I_{ref}, (red line), shown as a function of time.

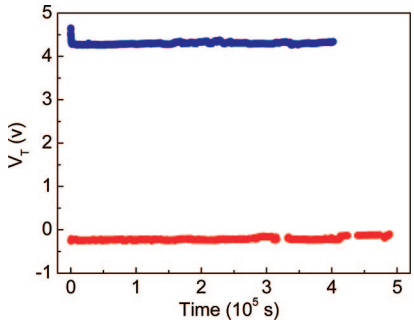

Figure 4. Fluctuation of gate threshold voltages, V_T, is shown as a function of time after a field-configurable transistor was configured to a low (red symbols) and a high (blue symbols) V_T value, respectively.

process was halted after I_d reached the preset I_{ref} value, and the device remained in the configured state until I_{ref} was reset to a different value to initiate another configuration cycle. The targeted configuration was carried out on three randomly selected FCTs, all of which were successfully configured to the targeted multiple states.

The nonvolatility of FCT devices was examined by monitoring the retention time of the configured FCT states. The FCTs were first configured to a high or low V_T state, then I_d was measured every 10 s for five days with low testing voltages of $V_d = 1$ V and $V_g = 0.5$ V. The V_T is derived from the measured I_d in transistor saturation and subthreshold regions for the low and high V_T states, respectively, and the variations of V_T are shown as a function of time in Figure 4. The fluctuation ranges of the V_T during the five day test are less than 0.25 V in both the high and low V_T states, indicating the reasonable nonvolatile nature of the FCTs.

To test the repeatability of the configuration, gate configuration-voltage pulses with a duration of 1 ms and magnitudes $V_g = 7$ and -5 V were applied alternately to configure the FCTs to the "high" and "low" I_d states, respectively, and reading pulses with a duration of 1 ms and magnitude $V_g =$ 1 V were then applied to read the state of the device. The FCTs were configured reversibly and repeatedly for more than $\sim 3 \times 10^5$ cycles with an on/off ratio of the drain−current about 1 order of magnitude before the measured device failed, probably due to a breakdown of the insulating gate SiO_2 layer.

The device configuration speeds were determined by varying the duration of the V_g pulse. A larger pulse amplitude was required in order to configure the FCTs effectively with a shorter pulse duration. The FCTs were successfully configured by pulses with a duration of 1 μs and an amplitude of 20 V. Any further decrease of the pulse duration would require a further increase of the pulse amplitude, which would likely induce electrical breakdown of the thin gate SiO_2 layer. Optimization of the gate structure should improve the configuration speed.

To understand the mechanism of the FCT configuration process, a two-terminal test device with the same Al/Ti/$RbAg_4I_5$/MEH-PPV/SiO_2/p-Si structure as the FCT gate shown in the Figure 1a was constructed and the change of the chemical composition in such test devices was investi-

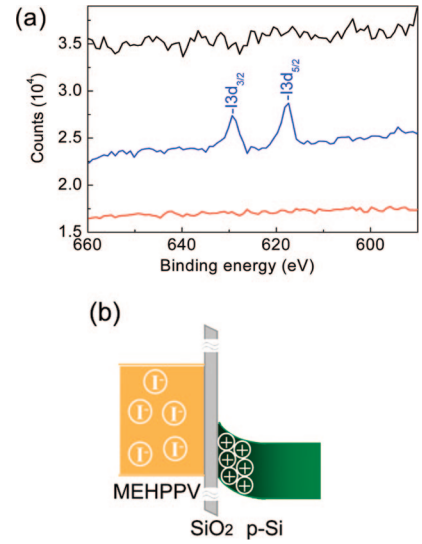

Figure 5. (a) XPS spectra of the I 3d region from the SiO_2 surfaces after the separation of the MEH-PPV/SiO_2 interface from the test devices configured by a positive gate bias of +4 V (red), a negative gate bias of −4 V (blue), and without configuration (black). (b) An energy band diagram of the MEH-PPV, SiO_2, and p-Si channel layers with iodide ions (marked as I^-) injected into the MEH-PPV layer and holes (marked as +) accumulated at the SiO_2/p-Si interface.

gated by X-ray photoelectron spectroscopy (XPS). The test devices used regular p-Si wafers with a boron dopant concentration of $\sim 5 \times 10^{15}$/cm^3 instead of the SOI wafers for the FCT devices and had a large area of ~ 3 mm^2 defined by its top metal electrode deposited through a shadow mask. A thick Al layer was deposited on the backside of the p-Si wafer as the bottom electric contact. The test devices were configured by applying positive or negative bias across the two electrodes. The chemical depth profile in the test devices was initially examined with XPS by ion-milling the multiple layers from the top electrode, but the difficulty to precisely control the ion-milling through the stacks of drastically different materials prevented the measurement of the depth profile. Utilizing a new procedure, the Al/Ti/$RbAg_4I_5$/MEH-PPV top layers were glued to a glass slide and then physically peeled off from the substrate to expose the SiO_2/p-Si surfaces, which were subsequently analyzed by XPS. As shown in Figure 5a, the presence of the I $3d_{3/2}$ and I $3d_{5/2}$ peaks of iodide anions in the XPS spectrum from the test device configured by applying a gate voltage of −4 V for 100 s clearly indicates that iodide anions were injected into the organic layer and driven all the way to the MEH-PPV/SiO_2 interface by the gate electric field. No iodine peaks were observed for the exposed SiO_2 surfaces for either devices without configuration or after applying a positive configuration voltage of 4 V for 100 s.

On the basis of the electronic measurements and the XPS results, we propose the following FCT configuration mechanism based on the electric field-driven modulation of iodide ions in the FCT gate region. When a large negative gate voltage $|V_g - (V_d + V_s)/2| > 1.5$ V is applied to the Al/Ti gate electrode, Ag cations in the $RbAg_4I_5$ ionic conductive layer are reduced, while iodide anions are injected from the

$RbAg_4I_5$ layer into the MEH-PPV polymer layer.[17,18] The iodide anions in the MEH-PPV layer drift toward the MEH-PPV/SiO_2 interface in the high electric field. The progressive increase of the anionic concentration near the MEH-PPV/SiO_2 interface induces the accumulation of holes in the p-type Si channel, resulting in the increase of the gate threshold voltage V_T of the FCT (Figure 5b). When a positive gate voltage $|V_g - (V_d + V_s)/2| > 1.5$ V is applied, the opposite process occurs, resulting in the decrease of V_T. During the configuration process, the $RbAg_4I_5$ ionic conductive layer functions as a source or sink of iodide anions for the MEH-PPV layer. When the FCT is operated as a FET with $|V_g - (V_d + V_s)/2| < 1.5$, the electrochemical processes are below threshold and the configured device state is nonvolatile. Compared with the configuration of electronic charge by electron tunneling in a floating gate FET, the configuration of the ionic charge in the FCT utilizes configuration voltages with much lower amplitude,[12] which enables the FCT to be configured more controllably, flexibly, and conveniently by modifying the number and amplitude of the configuration voltage pulses compatible with CMOS circuits. The conventional logic function of a floating gate FET has to be interrupted by the configuration process, but a FCT can be configured while functioning as a conventional FET. The simple double-layer gate structure of the FCT can also be conveniently integrated with different self-assembled nanowires. The analog configurability and plasticity of the FCT can potentially be used to correct variations of device characteristics and defects and provide defect tolerance in nanoscale integrated circuits.[8–11] Moreover, a circuit composed of dynamic field-configurable transistors can, in principle, be configured to arbitrary functions from external signals,[19] which may yield a synaptic electronic circuit with learning capability.

In summary, an organic/Si hybrid field-configurable transistor (FCT) has been fabricated on a Si nanowire FET platform. The gate threshold voltage of the FCT was configured to analog values ranging between −1 V and +4 V precisely, dynamically, repeatedly, and reversibly by adjusting the amplitude, polarity, and duration of a configuration gate voltage pulse V_g with $|V_g - (V_d + V_s)/2| > 1.5$ V. The FCT is nonvolatile and can operate as a conventional Si FET as long as $|V_g - (V_d + V_s)/2| < 1.5$ V. We are exploring the fabrication and demonstration of a defect-tolerant nanoelectronic circuit and a synaptic electronic circuit with dynamic learning functions based on FCTs.

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Supporting Information Available: Closed-loop feedback circuit for targeted configuration; characteristics of a Si field effect transistor as control. This material is available free of charge via the Internet at http://pubs.acs.org.

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